

**MEMORY CIRCUIT AND MEMORIZATION OF DATA STREAM****Publication number:** JP1266593 (A)**Publication date:** 1989-10-24**Inventor(s):** MASASHI HASHIMOTO; JIIN EI FURANTSU; JIYON  
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G09G1/02; H04N5/91***- European:****Application number:** JP19880324738 19881222**Priority number(s):** US19870137305 19871223**Also published as:**

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**Abstract of JP 1266593 (A)**

**PURPOSE:** To attain efficiency in the special effect of a video device by enabling both serial access and random access to be executed and executing the initial setting of a series of memory addresses which are generated by means of an address sequencer. **CONSTITUTION:** A memory circuit 14 can perform both serial access and random access. The datainput of random access memory array 24 is connected to a data buffer and the data buffer synchronizes the operation of memory array 24 with a data stream. The address input of memory array 24 is connected to the address sequencer 40a and the series of memory addresses which are impressed on memory array 24 are generated.; Moreover, an address buffer register 36a is connected to the address sequencer 40a, a random access address is supplied to the address sequencer 40a and the memory address supplied from the address sequencer 40a is initially set. Thus, a system is efficiently used in the wide-range of video usage of the special effect.

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